Amendments of the Claims:

A detailed listing of all claims in the application is presented below. This listing of claims will replace all prior versions, and listings, of claims in the application. All claims being currently amended are submitted with markings to indicate the changes that have been made relative to immediate prior version of the claims. The changes in any amended claim are being shown by strikethrough (for deleted matter) or underlined (for added matter).

1. (Currently Amended) A semiconductor device comprising a substrate, a plastically relaxed layer grown on top of the substrate wherein a thickness of the plastically relaxed layer exceeds a critical thickness for plastic strain relaxation, and a defect–free layer grown on top of the plastically relaxed layer;

~~The semiconductor device of claim 43,~~ wherein at least a part of the device is manufactured by a method of fabrication of defect–free epitaxial layers on top of a surface of the plastically relaxed layer having a first thermal evaporation rate and a plurality of defects, wherein the surface comprises at least one defect-free surface region, and at least one surface region in a vicinity of the defects, the method comprising the steps of:

a) depositing a cap layer comprising a second material having a second thermal evaporation rate different from the first thermal evaporation rate, wherein the cap layer is selectively deposited on the defect–free surface region, such that at least one of the regions of the surface in the vicinity of the defects remains uncovered;

b) annealing a structure created in step a) at a temperature and duration such that at least one of the surface regions in the vicinity of the defects that is uncovered evaporates, while defect-free surface regions covered by the cap layer remain unaffected, and at least one annealed region is formed; and

c) depositing a third material, lattice–matched or nearly lattice matched to the plastically relaxed layer, such that the third material overgrows both the cap layer and annealed regions of the plastically relaxed layer forming the defect-free-layer.

2. (Original) The semiconductor device of claim 1, wherein the device is selected from the group consisting of:

a) a high electron mobility transistor;

b) a field effect transistor;

c) a heterojunction bipolar transistor; and

d) an integrated circuit.

3. (Original) The semiconductor device of claim 1, wherein the device is selected from the group consisting of:

a) a diode laser;

b) a light-emitting diode;

c) a photodetector;

d) an optical amplifier;

e) a far infrared intraband detector;

f) an intraband far infrared emitter;

g) a resonant tunneling diode;

h) a solar cell; and

i) an optically bistable device.

4. (Original) The semiconductor device of claim 1, wherein the device is selected from the group consisting of:

a) a current-injection edge-emitting laser;

b) a vertical cavity surface emitting laser; and

c) a tilted cavity laser.

5. (Previously Presented) The semiconductor device of claim 1, wherein the plastically relaxed layer is a defect–containing epitaxial layer.

6. (Original) The semiconductor device of claim 1, wherein at least one defect is a propagating defect selected from the group consisting of:

a) at least one threading dislocation;

b) at least one screw dislocation;

c) at least one stacking fault;

d) at least one antiphase boundary; and

e) any combination of a) through d).

7. (Original) The semiconductor device of claim 1, wherein the defects comprise at least one local defect which causes a propagating defect in a subsequently deposited epitaxial layer.

8. (Original) The semiconductor device of claim 7, wherein the local defect is selected from the group consisting of:

a) at least one local dislocation;

b) at least one misfit dislocation;

c) at least one local defect dipole;

d) at least one dislocation network;

e) at least one dislocation loop;

f) at least one dislocated cluster;

g) at least one impurity precipitate;

h) at least one oval defect;

i) a plurality of dirt particles on the surface; and

j) any combination of a) through i).

9. (Original) The semiconductor device of claim 1, wherein step (a) of the method comprises a deposition process selected from the group consisting of:

a) molecular beam epitaxy deposition;

b) metal-organic chemical vapor deposition; and

c) vapor phase epitaxy deposition.

10. (Original) The semiconductor device of claim 1, wherein step (c) of the method comprises a deposition process selected from the group consisting of:

a) molecular beam epitaxy deposition;

b) metal-organic chemical vapor deposition; and

c) vapor phase epitaxy deposition.

11. (Original) The semiconductor device of claim 1, wherein steps (a) and (b) of the method are repeated two times to twenty times.

12. (Original) The semiconductor device of claim 1, wherein steps (a) through (c) of the method are repeated two times to forty times.

13. (Original) The semiconductor device of claim 1, wherein the surface region in the vicinity of the defects differs from the defect-free surface region in a strain state, such that the cap layer is repelled from and does not cover the surface region in the vicinity of the defects.

14. (Original) The semiconductor device of claim 1, wherein the surface region in the vicinity of the defects differs from the defect-free surface region in a surface energy, such that the

cap layer is repelled from and does not cover the surface region in the vicinity of the defects.

15. (Original) The semiconductor device of claim 1, wherein the surface region in the vicinity of the defects differs from the defect-free surface region in a surface stress, such that the cap layer is repelled from and does not cover the surface region in the vicinity of the defects.

16. (Original) The semiconductor device of claim 1, wherein the surface region in the vicinity of the defects differs from the defect-free surface region in a surface morphology, such that the cap layer is repelled from and does not cover the surface region in the vicinity of the defects.

17. (Original) The semiconductor device of claim 1, wherein the surface region in the vicinity of the defects differs from the defect-free surface region in wetting/non-wetting properties with respect to the deposition of the cap layer material, such that the cap layer is repelled from and does not cover the surface region in the vicinity of the defects.

18. (Original) The semiconductor device of claim 1, wherein an evaporation of the defect-containing regions is enhanced by chemical etching using a flux of chemically–active particles, wherein the chemically–active particles are selected from the group consisting of:

a) atoms;

b) molecules; and

c) ions.

19. (Original) The semiconductor device of claim 1, wherein an evaporation of the defect-containing regions is enhanced by a plasma etching process.

20. (Original) The semiconductor device of claim 1, wherein an evaporation of the defect-containing regions is enhanced by a wet etching process.

21. (Previously Presented) The semiconductor device of claim 1, wherein the thermal annealing in step (b) of the method results in the formation of troughs at a plurality of exits of the defects in the plastically relaxed layer.

22. (Original) The semiconductor device of claim 1, wherein the growth of the second epitaxial layer occurs in the lateral epitaxial overgrowth mode.

23. (Previously Presented) The semiconductor device of claim 22, wherein step (c) of the method comprises the substeps of:

a) starting growth of the third material at the surface regions covered by the cap layer;

b) continuing the growth of the third material in a lateral plane resulting in merging of neighboring domains of lateral epitaxial overgrowth; and

c) forming the defect-free layer from the third material, wherein the defect-free layer is suitable for further epitaxial growth.

24. (Original) The semiconductor device of claim 1, wherein at least one void remains in the third material.

25. (Original) The semiconductor device of claim 1, wherein no voids remain in the third material.

26. (Previously Presented) The semiconductor device of claim 1, wherein the method further comprises the step of, prior to step (a), the deposition of a fourth material, lattice–matched or nearly lattice–matched to the plastically relaxed layer, wherein the fourth material provides a repulsion of the second material of the cap layer from defect-containing surface regions.

27. (Previously Presented) The semiconductor device of claim 1, wherein the method further comprises the step of, prior to step (a), the deposition of a fourth material, wherein the fourth material is in a no-strain state lattice–mismatched to the plastically relaxed layer, wherein a thickness of the fourth material is below a critical thickness required for a

creation of new defects, such that the fourth material forms a strained defect-free thin pseudomorphic layer.

28. (Original) The semiconductor device of claim 27, wherein the pseudomorphic layer provides a repulsion of the second material of the cap layer from defect-containing surface regions.

29. (Currently Amended) A semiconductor device comprising a substrate, a plastically relaxed layer grown on top of the substrate wherein a thickness of the plastically relaxed layer exceeds a critical thickness for plastic strain relaxation, and a defect–free layer grown on top of the plastically relaxed layer;

~~The semiconductor device of claim 43,~~ wherein at least a part of the device is manufactured by a method of fabrication of defect–free epitaxial layers on a surface of the plastically relaxed layer, the method comprising the steps of:

a) depositing the plastically relaxed layer having a first thermal evaporation rate, wherein the plastically relaxed layer is lattice-mismatched to a substrate, wherein a thickness of the plastically relaxed layer exceeds a critical thickness required for a formation of defects, such that a plurality of defects are formed in the plastically relaxed layer, wherein the surface of the plastically relaxed layer comprises at least one defect-free surface region, and at least one surface region in a vicinity of the defects;

b) depositing a cap layer of a second material having a second thermal evaporation rate different from the first thermal evaporation rate, such that the cap layer is selectively deposited on the defect–free surface regions, and at least one of the surface regions in the vicinity of the defects remains uncovered;

c) annealing a structure formed in step b) at a temperature and duration such that at least one of the surface regions in the vicinity of the defects that is uncovered evaporates, while defect-free surface regions covered by the cap layer remain unaffected, and at least one annealed region is formed; and

d) depositing a third material, lattice–matched or nearly lattice matched to the first epitaxial layer, such that the third material overgrows both the cap layer and annealed regions of the first epitaxial layer, forming the~~a~~ defect-free ~~epitaxial~~ layer suitable as a template for further epitaxial growth.

30. (Currently Amended) The semiconductor device of claim 1~~43~~, wherein the device is a high electron mobility transistor and:

a) the substrate is selected from the group consisting of a Si substrate and a GaAs substrate;

b) the plastically relaxed layer is a plastically relaxed $Ga_{1-x}In_xAs$ layer; and

c) the defect-free layer is a defect–free $Ga_{1-y}In_yAs$ layer.

31. (Currently Amended) The semiconductor device of claim 1~~43~~, wherein the device is a high electron mobility transistor and:

a) the substrate is selected from the group consisting of a Si substrate and a GaAs substrate;

b) the plastically relaxed layer is a plastically relaxed $Ga_{1-x}In_xAs$ layer; and

c) the defect-free layer is a defect–free $Ga_{1-y-z}In_yAl_zAs$ layer.

32. (Currently Amended) The semiconductor device of claim 1~~43~~, wherein the device is a high electron mobility transistor and:

a) the substrate is selected from the group consisting of a Si substrate with a surface orientation (111), a SiC substrate, and a sapphire substrate;

b) the plastically relaxed layer is a plastically relaxed GaN layer; and

c) the defect-free layer is a defect–free GaN layer.

33. (Currently Amended) The semiconductor device of claim 1~~43~~, wherein the device is a high electron mobility transistor and:

a) the substrate is selected from the group consisting of a Si substrate with a surface orientation (111), a SiC substrate, and a sapphire substrate;

b) the plastically relaxed layer is a plastically relaxed $Ga_{1-x}In_xN$ layer; and

c) the defect-free layer is a defect–free $Ga_{1-y}In_yN$ layer.

34. (Currently Amended) The semiconductor device of claim 1~~43~~, wherein the device is an integrated circuit and:

a) the substrate is a Si substrate;

b) the plastically relaxed layer is a plastically relaxed $Si_{1-x}Ge_x$ layer;

c) the defect-free layer is a defect–free $Si_{1-y}Ge_y$ layer;

wherein the device further comprises a thin pseudomorphically strained Si layer grown on top of the defect–free $Si_{1-y}Ge_y$ layer.

35. (Currently Amended) The semiconductor device of claim 1~~43~~, wherein the device is a tilted cavity laser grown on an GaAs substrate, further comprising an epitaxial layer comprising a material selected from the group consisting of GaAs and $Ga_{1-z}Al_zAs$;

wherein the plastically relaxed layer is a plastically relaxed $Ga_{1-x}In_xAs$ layer grown on top of the epitaxial layer;

wherein the defect-free layer is a $Ga_{1-y}In_yAs$ layer grown on top of the plastically relaxed $Ga_{1-x}In_xAs$ layer; and

wherein an n-part of a cavity comprises the epitaxial layer, the plastically relaxed layer, and the defect-free layer.

36. (Previously Presented) The device of claim 35, wherein the laser generates laser light in the wavelength region of 1.4 through 1.8 micrometers.

37.(Currently Amended) ~~The device of claim 43, wherein the device is~~ A GaN-based vertical cavity surface emitting laser ~~further~~ comprising a cavity comprising a substrate, a

plastically relaxed layer grown on top of the substrate wherein a thickness of the plastically relaxed layer exceeds a critical thickness for plastic strain relaxation, and a defect–free layer grown on top of the plastically relaxed layer, wherein at least a part of the cavity is made by a method comprising the steps of:

a) depositing the ~~a~~ plastically relaxed layer having a first thermal evaporation rate on the ~~a~~ substrate, wherein the plastically relaxed layer is lattice-mismatched to the substrate, wherein a thickness of the plastically relaxed layer exceeds a critical thickness required for a formation of defects, such that a plurality of defects are formed in the plastically relaxed layer, such that a surface of said plastically relaxed layer comprises at least one defect-free surface region, and at least one surface region in a vicinity of the defects;

b) depositing a cap layer of a second material having a second thermal evaporation rate different from the first thermal evaporation rate, such that the cap layer is selectively deposited on the defect–free surface regions, and at least one of the surface regions in the vicinity of the defects remains uncovered;

c) annealing a structure formed in step b) at a temperature and duration such that at least one of the surface regions in the vicinity of the defects that is uncovered evaporates, while defect-free surface regions covered by the cap layer remain unaffected, and at least one annealed region is formed; and

d) depositing a third material, lattice–matched or nearly lattice matched to the first epitaxial layer, such that the third material overgrows both the cap layer and annealed regions of the first epitaxial layer, forming the defect-free layer suitable as a template for further epitaxial growth.

38. (Previously Presented) The device of claim 37, wherein the laser generates laser light in a wavelength region from 100 nanometers to 600 nanometers.

39. (Currently Amended) ~~The semiconductor device of claim 43, wherein the device is a~~ A GaN-based edge-emitting laser comprising a waveguide comprising a substrate, a plastically relaxed layer grown on top of the substrate wherein a thickness of the plastically relaxed

layer exceeds a critical thickness for plastic strain relaxation, and a defect–free layer grown on top of the plastically relaxed layer, wherein at least a part of the waveguide is made by a method comprising the steps of:

a) depositing the plastically relaxed layer having a first thermal evaporation rate on thea substrate, wherein the plastically relaxed layer is lattice-mismatched to the substrate, wherein a thickness of the plastically relaxed layer exceeds a critical thickness required for a formation of defects, such that a plurality of defects are formed in the plastically relaxed layer, such that a surface of said plastically relaxed layer comprises at least one defect-free surface region, and at least one surface region in a vicinity of the defects;

b) depositing a cap layer of a second material having a second thermal evaporation rate different from the first thermal evaporation rate, such that the cap layer is selectively deposited on the defect–free surface regions, and at least one of the surface regions in the vicinity of the defects remains uncovered;

c) annealing a structure formed in step b) at a temperature and duration such that at least one of the surface regions in the vicinity of the defects that is uncovered evaporates, while defect-free surface regions covered by the cap layer remain unaffected, and at least one annealed region is formed; and

d) depositing a third material, lattice–matched or nearly lattice matched to the plastically relaxed layer, such that the third material overgrows both the cap layer and annealed regions of the plastically relaxed layer, forming the defect-free layer suitable as a template for further epitaxial growth.

40. (Previously Presented) The device of claim 39, wherein the laser generates laser light in a wavelength region from 100 nanometers to 600 nanometers.

41. (Currently Amended) AThe device of claim 43, wherein the device is a GaN-based tilted cavity laser further comprising a cavity comprising a substrate, a plastically relaxed layer grown on top of the substrate wherein a thickness of the plastically relaxed layer exceeds a critical thickness for plastic strain relaxation, and a defect–free layer grown on top of

the plastically relaxed layer, wherein at least a part of the cavity is made by a method comprising the steps of:

a) depositing the plastically relaxed layer having a first thermal evaporation rate on thea substrate, wherein the plastically relaxed layer is lattice-mismatched to the substrate, wherein a thickness of the plastically relaxed layer exceeds a critical thickness required for a formation of defects, such that a plurality of defects are formed in the plastically relaxed layer, such that a surface of said plastically relaxed layer comprises at least one defect-free surface region, and at least one surface region in a vicinity of the defects;

b) depositing a cap layer of a second material having a second thermal evaporation rate different from the first thermal evaporation rate, such that the cap layer is selectively deposited on the defect–free surface regions, and at least one of the surface regions in the vicinity of the defects remains uncovered;

c) annealing a structure formed in step b) at a temperature and duration such that at least one of the surface regions in the vicinity of the defects that is uncovered evaporates, while defect-free surface regions covered by the cap layer remain unaffected, and at least one annealed region is formed; and

d) depositing a third material, lattice–matched or nearly lattice matched to the plastically relaxed layer, such that the third material overgrows both the cap layer and annealed regions of the plastically relaxed layer, forming the defect-free layer suitable as a template for further epitaxial growth.

42. (Previously Presented) The device of claim 41, wherein the laser generates laser light in the wavelength region from 100 nanometers to 600 nanometers.

43. (Cancelled)